AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

LISTING OF CLAIMS:

1. (Currently Amended) A semiconductor storage apparatus to be coupled with a system bus to receive a write request accompanied with first and second ~~blocks~~ sectors of data, comprising;

a plurality of nonvolatile semiconductor memories which store said first and second ~~blocks~~ sectors of data therein; and

a control ~~means~~ module to be coupled with said system bus, and coupled with said plurality of nonvolatile semiconductor memories,

wherein said control ~~means~~ module sends a first erase command to one of said plurality of nonvolatile semiconductor memories to initiate a first internal erase operation of data within said one of said plurality of nonvolatile semiconductor memories, and

wherein, after said first erase command has been sent, said control ~~means~~ module sends a second erase command to another of said plurality of nonvolatile semiconductor memories, different from said one of said plurality of nonvolatile semiconductor memories to which said first erase command was sent ~~and which is under said first internal erase operation,~~ to initiate a second internal erase operation of data within said other of said plurality of nonvolatile semiconductor memories while said one of said plurality of nonvolatile semiconductor memories is still performing said first internal erase operation responsive to said first erase command.

2. (Currently Amended) A semiconductor storage apparatus according to claim 1, farther comprising:

a buffer memory, coupled commonly with said plurality of nonvolatile semiconductor memories, which holds said first and second ~~blocks~~ sectors of data as write data to be written into said plurality of nonvolatile semiconductor memories,

wherein said control ~~means~~ module responds to said write request, carries out read operations of said first and second ~~blocks~~ sectors of data as said write data from said buffer memory and carries out write operations of said first and second ~~blocks~~ sectors of data as said write data read out from said buffer memory into said plurality of nonvolatile semiconductor memories, wherein said write operations into said plurality of nonvolatile semiconductor memories are controlled by sending a first write command from said control ~~means~~ module to one of said plurality of nonvolatile semiconductor memories and by sending a second write command from said control ~~means~~ module to another of said plurality of nonvolatile semiconductor memories different from said one to which said first write command has been sent ~~and which is under a write operation responsive to said first write command~~while said one of said plurality of nonvolatile semiconductor memories is still performing a write operation responsive to said first write command.

3. (Original) A semiconductor storage apparatus according to claim 1, wherein each of said plurality of nonvolatile semiconductor memories is comprised of a flash memory semiconductor chip.

4. (Original) A semiconductor storage apparatus according to claim 2, wherein each of said plurality of nonvolatile semiconductor memories is comprised of a flash memory semiconductor chip.

5. (Original) A semiconductor storage apparatus according to claim 2, wherein said buffer memory has a storage memory capacity corresponding to a plurality of sectors in units of 512 bytes which is a sector capacity of a standard disk.

6. (Currently Amended) A semiconductor storage apparatus according to claim 1, wherein said control ~~means~~ module includes a processor.

7. (Currently Amended) A semiconductor storage apparatus according to claim 2, wherein said control ~~means~~ module includes a processor

8. (Currently Amended) A semiconductor storage apparatus according to claim 1, wherein said control ~~means~~ module further includes an address controller.

9. (Currently Amended) A semiconductor storage apparatus according to claim 2, wherein said control ~~means~~ module further includes an address controller,

10. (Original) A semiconductor storage apparatus according to claim 1, wherein each of said plurality of nonvolatile semiconductor memories is comprised of a flash memory semiconductor chip, and wherein said buffer memory has a storage memory capacity corresponding to a plurality of sectors in units of 512 bytes which is a sector capacity of a standard disk.

11. (Original) A semiconductor storage apparatus according to claim 2, wherein each of said plurality of nonvolatile semiconductor memories is comprised of a flash memory semiconductor chip, and

wherein said buffer memory has a storage memory capacity corresponding to a plurality of sectors in units of 512 byte which is a sector capacity of a standard disk.

12. (Currently Amended) A semiconductor storage apparatus according to claim 10, wherein said control ~~means~~ module includes a processor.

13. (Currently Amended) A. semiconductor storage apparatus according to claim 11, wherein said control ~~means~~ module includes a processor.

14. (Currently Amended) A semiconductor storage apparatus according to claim 10, wherein said control ~~means~~ module further includes an address controller.

15. (Currently Amended) A semiconductor storage apparatus according to claim 11, wherein said control ~~means~~ module further includes an address controller.

16. (New) A semiconductor storage apparatus to be coupled with a system bus comprising:

a plurality of nonvolatile semiconductor memories which write data from said system therein in sector units and erase said data in block units, said each block including a plurality of said sectors; and

a control module to be coupled with said system bus, and coupled with said plurality of nonvolatile semiconductor memories,

wherein said control module sends a first erase command to one of said plurality of nonvolatile semiconductor memories to initiate a first internal erase

operation of data in said block units within said one of said plurality of nonvolatile semiconductor memories, and

wherein, after said first erase command has been sent, said control module sends a second erase command to an other of said plurality of nonvolatile semiconductor memories, different from said one of said plurality of nonvolatile semiconductor memories to which said first erase command was sent, to initiate a second internal erase operation of data in said block units within said other of said plurality of nonvolatile semiconductor memories while said one of said plurality of nonvolatile semiconductor memories is still performing said first internal erase operation responsive to said first erase command.

17. (New) A semiconductor storage apparatus according to claim 16, wherein said control module carries out a status polling operation in an order of said nonvolatile semiconductor memories to which said control module sent said erase commands, after said control module sent said erase commands to all of said nonvolatile semiconductor memories.